an array processor for performing arithmetic calculations, the array processor coupled to the interface circuit to receive information therefrom and connected to the embedded processor via an internal bus; and

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands; and

a first shared operand unit coupled to the first MAC unit and the second MAC unit for providing a first shared operand to the first MAC unit for computing a first result in association with the first plurality of operands and to the second MAC unit for computing a second result in association with the second plurality of operands; and

wherein the first result and the second result are computed independently of each other; and

wherein the array processor further comprises:

a second shared operand unit coupled to a third MAC unit and a forth MAC unit for providing a second shared operand to the third MAC unit and the forth MAC unit.

3. The integrated circuit according to claim 1 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and said array processor, and wherein said wire bundle comprises at least 256 wires.

10. An integrated circuit using a memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

a embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits; and

a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for providing a shared operand to at least two of said plurality of multiplier/accumulator circuits.

11. The integrated circuit according to claim 10 wherein said interface circuit includes a wire bundle for providing wide access data transfers between the interface and said array processor, and wherein said wire bundle comprises at least 256 wires.

12. The integrated circuit according to claim 10 wherein separate instruction and data streams are maintained for said array processor.

13. The integrated circuit according to claim 10 wherein separate instruction and data streams are maintained for said embedded processor.

14. The integrated circuit according to claim 10 wherein said interface circuit is a Master Memory Interface Controller (MMIC) circuit.

15. The integrated circuit according to claim 10 wherein a multiplier/accumulator circuit of said plurality of multiplier/accumulator circuits comprises a computational unit that multiplies a first operand by a second operand to obtain a result and then adds or subtracts from said result a third operand, wherein said operands are either scalars or vectors.

16. The integrated circuit according to claim 10 further comprising a global external bus unit for providing an interface between said integrated circuit and said external environment, said global external bus unit coupled to said embedded microprocessor by a system bus and by a separate dedicated bus.

17. The integrated circuit according to claim 10 wherein said array processor performs a plurality of vector operations selected from a group consisting of addition of a plurality of vectors and multiplying a vector by a scalar.

18. The integrated circuit according to claim 10 wherein said array processor is configured to share a plurality of scalar elements among a plurality of vector components of a vector, wherein a first scalar element of said plurality of scalar elements mathematically operating on a first vector component of said plurality of vector components and a second scalar element of

said plurality of scalar elements mathematically operating on a second vector component of said plurality of vector components are calculated in parallel.

19. The integrated circuit according to claim 10 wherein said array processor uses a simplified IEEE floating point notation which excludes said IEEE floating point exceptions, comprising underflow, overflow, divide by zero, inexact, and invalid.

20. The array processor of claim 10 further comprising:

a front end unit for determining a fixed point result by performing a fixed point addition or subtraction on a plurality of operands;

a floating point conversion unit for converting said fixed point result to a first floating point result; and

a multiplier and accumulator unit for determining a second floating point result by performing a floating point multiplication and then accumulation using at least said first floating point result.

21. An integrated circuit for image frame rendering applications, said integrated circuit during operation operating with memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

a processor embedded in said integrated circuit, said processor receiving information from said interface circuit; and

an array processor coupled to said interface circuit and to said processor via an internal bus;

wherein the array processor is configured to:

determine a fixed point result by performing a fixed point addition or subtraction on a plurality of fixed point operands;

convert the fixed point result to a first floating point result; and

determine a second floating point result by performing a floating point multiplication and then accumulation using the first floating point result and at least one floating point operand.

22. The integrated circuit according to claim 21 wherein said array processor comprises: